

What is claimed is:

1           1. A method for forming active regions of field effect transistors, comprising:

2           (a) forming at least one conductive region over an isolation layer formed on a substrate,  
3 and a cap dielectric layer on the at least one conductive region;

4           (b) forming a sacrificial dielectric layer over the isolation layer and the cap dielectric  
5 layer, and on sidewalls of the at least one conductive region;

6           (c) removing a portion of the sacrificial dielectric layer on the cap dielectric layer;

7           (d) removing the cap dielectric layer; and

8           (e) removing remaining portions of the sacrificial dielectric layer.

1           2. The method of claim 1, wherein the cap dielectric layer includes a first cap dielectric  
2 layer and a second cap dielectric layer.

1           3. The method of claim 2, wherein step (d) comprises the step of removing the first cap  
2 dielectric layer and the second cap dielectric layer.

1           4. The method of claim 3, wherein the sacrificial dielectric layer is formed to a thickness  
2 at least larger than a thickness loss caused by removing the first cap dielectric layer and the  
3 second cap dielectric layer.

1           5. The method of claim 1, further comprising performing a sputtering step to trim the  
2 remaining portions of the sacrificial dielectric layer prior to removal thereof.

1           6. The method of claim 1, wherein the at least one conductive region has a mesa  
2 structure.

1           7. The method of claim 1, wherein the sacrificial dielectric layer is formed to a thickness  
2 at least larger than a thickness loss caused by step (d).

1           8. The method of claim 1, wherein step (c) is performed by a chemical mechanical polish  
2 (CMP) process with a high selectivity slurry.

1           9. The method of claim 8, wherein the CMP process with the high selectivity slurry has  
2 different removing rates for different regions of the sacrificial dielectric layer in response to  
3 different polish pressures applied thereto.

1           10. The method of claim 9, wherein the high selectivity slurry comprises a ceria-based  
2 abrasive and an electronegative surfactant.

1           11. The method of claim 1; further comprising the step of performing a cleaning process  
2 after step (d), wherein said sacrificial dielectric layer has a thickness during said cleaning process  
3 sufficient to substantially protect said at least one conductive region from undercut in the  
4 isolation layer.

1           12. A method for forming active regions of field effect transistors, comprising:

2           (a) forming at least one conductive mesa over an isolation layer formed on a substrate,  
3 and a cap dielectric layer on the at least one conductive mesa;

4           (b) forming a sacrificial dielectric layer over the isolation layer and the cap dielectric  
5 layer, and on sidewalls of the at least one conductive mesa;

6           (c) removing a portion of the sacrificial dielectric layer on the cap dielectric layer by a  
7 chemical mechanical polish (CMP) process with a high selectivity slurry;

8           (d) removing the cap dielectric layer, wherein the sacrificial dielectric layer is formed to a  
9 thickness at least larger than a thickness loss caused by removal step (d); and

10          (e) removing remaining portions of the sacrificial dielectric layer.

1           13. The method of claim 12, wherein the cap dielectric layer includes a first cap dielectric  
2 layer and a second cap dielectric layer.

1           14. The method of claim 13, wherein step (d) comprises the step of removing the first cap  
2 dielectric layer and the second dielectric layer.

1           15. The method of claim 14, wherein the sacrificial dielectric layer is formed to a  
2 thickness at least larger than a thickness loss caused by removing the first cap dielectric layer and  
3 the second cap dielectric layer.

1           16. The method of claim 12, further comprising performing a sputtering step to trim the  
2 remaining portions of the sacrificial dielectric layer prior to removal thereof.

1           17. The method of claim 12, wherein the CMP process with the high selectivity slurry has  
2 different removing rates for different regions of the sacrificial dielectric layer in response to  
3 different polish pressures applied thereto.

1           18. The method of claim 17, wherein the high selectivity slurry comprises a ceria-based  
2 abrasive and an electronegative surfactant.

1           19. A method for forming field effect transistors, comprising:  
2           (a) forming at least one conductive mesa over an isolation layer formed on a substrate,  
3 and a cap dielectric layer on the at least one conductive mesa;  
4           (b) forming a sacrificial dielectric layer over the isolation layer and the cap dielectric  
5 layer, and on sidewalls of the at least one conductive mesa;  
6           (c) removing a portion of the sacrificial dielectric layer on the cap dielectric layer by a  
7 chemical mechanical polish (CMP) process with a high selectivity slurry;  
8           (d) removing the cap dielectric layer;  
9           (e) removing remaining portions of the sacrificial dielectric layer;  
10          (f) forming a gate on the at least one conductive region; and  
11          (g) forming source/drain (S/D) regions within the at least one conductive region and  
12 adjacent to the gate.

1           20. The method of claim 19, wherein the cap dielectric layer includes a first cap dielectric  
2 layer and a second cap dielectric layer.

1           21. The method of claim 20, wherein step (d) comprises the step of removing the first cap  
2 dielectric layer and the second dielectric layer.

1           22. The method of claim 21, wherein the sacrificial dielectric layer is formed to a  
2 thickness at least larger than a thickness loss caused by removing the first cap dielectric layer and  
3 the second cap dielectric layer.

1           23. The method of claim 19, further comprising performing a sputtering step to trim the  
2 remaining portions of the sacrificial dielectric layer prior to removal thereof.

1           24. The method of claim 19, wherein the at least one conductive region has a mesa  
2 structure.

1           25. The method of claim 19, wherein the sacrificial dielectric layer is formed to a  
2 thickness at least larger than a thickness loss caused by step (d).

1           26. The method of claim 19, wherein step (c) is performed by a chemical mechanical  
2 polish (CMP) process with a high selectivity slurry.

1           27. The method of claim 26, wherein the CMP process with the high selectivity slurry has  
2 different removing rates for different regions of the sacrificial dielectric layer in response to  
3 different polish pressures applied thereto.

1           28. The method of claim 27, wherein the high selectivity slurry comprises a ceria-based  
2 abrasive and an electronegative surfactant.

1           29. An integrated circuit including a field effect transistor, the field effect transistor  
2 comprising:  
3           a conductive region on a substrate having an isolation layer formed thereon, the isolation  
4 layer being substantially without undercut at the region within the isolation layer beneath the  
5 conductive region;

6 a gate on the conductive region; and  
7 source/drain (S/D) regions within the conductive region and adjacent to the gate.

1 30. The integrated circuit of claim 29, wherein any undercut within the isolation layer  
2 beneath the conductive region has a lateral depth no more than about 100Å.

1 31. The integrated circuit of claim 29, wherein the conductive region has a mesa  
2 structure.

1 32. An integrated circuit including a plurality field effect transistors having active regions  
2 formed by the process of claim 1.

1 33. A method for forming field effect transistors, comprising:  
2 (a) forming at least one conductive region over an isolation layer formed on a substrate;  
3 (b) forming a sacrificial dielectric layer over the isolation layer and adjacent to said at  
4 least one conductive region;  
5 (c) forming a gate dielectric layer over said at least one conductive region, and  
6 (d) performing a cleaning process prior to forming said gate dielectric layer, wherein said  
7 sacrificial dielectric layer is formed to a thickness sufficient to substantially protect said at least  
8 one conductive region from undercut in the isolation layer from said cleaning process.

1 34. The method of claim 33, wherein said cleaning process utilizes a HF solution.